ABSTRACT

In some embodiments, a method and apparatus for an energy efficient clustered micro-architecture are disclosed. In one embodiment, the method includes the computation of an energy delay^2 product for each active instruction scheduler and one or more associated function blocks of a current architecture configuration over a predetermined period. Once the energy delay^2 product is computed, the computed product is compared against an energy delay^2 product calculated for a prior architecture configuration to determine an effectiveness of the current architecture configuration. Based on the effectiveness of the current architecture configuration, a number of active instruction schedulers and one or more associated functional blocks within the current architecture configuration is adjusted. In one embodiment, the number of active instruction schedulers and one or more associated functional blocks may be increased or decreased to improve power efficiency of the cluster micro-architecture. Other embodiments are described and claimed.